WHAT IS CLAIMED IS:

1. An ESD protection circuit of a non-gated diode coupled between an input pad and an internal circuit, comprising:

a high-voltage supply rail and a low-voltage supply rail;

a first diode, with an anode coupled to the high-voltage supply rail and a cathode coupled to a node;

a second diode, with a cathode coupled to the low-voltage supply rail and an anode coupled to the node;

a first diode series, having a plurality of serially connected diodes, wherein an anode thereof is coupled to the high-voltage supply rail and a cathode thereof is coupled to the node; and

a second diode series, having a plurality of serially connected diodes, wherein a cathode thereof is coupled to the low-voltage supply rail and an anode thereof is coupled to the node.

2. The ESD protection circuit according to claim 1, wherein when a voltage positive relative to the high-voltage supply rail is applied to the input pad, the ESD protection circuit provides a discharge path from the first diode to the high-voltage supply rail.

3. The ESD protection circuit according to claim 1, wherein when a voltage negative relative to the low-voltage supply rail is applied to the input pad, the ESD protection circuit provides a discharge path from the second diode to the low-voltage supply rail.

4. The ESD protection circuit according to claim 1, wherein when a voltage negative relative to the high-voltage supply rail is applied to the input pad, the ESD

protection circuit provides a discharge path from the second diode, the second diode series and the first diode series to the high-voltage supply rail.

5. The ESD protection circuit according to claim 1, wherein when a voltage positive relative to the low-voltage supply rail is applied to the input pad, the ESD protection circuit provides a discharge path from the first diode, the first diode series and the second diode series to the low-voltage supply rail.

6. The ESD protection circuit according to claim 1, wherein each of the first diode, the second diode, the first diode series and the second diode series includes a non-gate diode formed by SOI fabrication process.

7. The ESD protection circuit according to claim 1, wherein each of the first diode, the second diode, the first diode series and the second diode series includes a non-gate diode formed by bulk CMOS fabrication process.

8. The ESD protection circuit according to claim 1, wherein the first and second diodes have the same dimension and the same junction capacitance.

9. The ESD protection circuit according to claim 1, wherein the first and second diodes have different dimensions and the different junction capacitances.

10. An ESD protection circuit of a non-gated diode, coupled between an output pad and a pre-driver, comprising:

a high-voltage supply rail and a low-voltage supply rail, coupled to the pre-driver;

a first diode, with an anode coupled to the high-voltage supply rail and a cathode coupled to a node;

a second diode, with a cathode coupled to the low-voltage supply rail and an anode coupled to the node;

a first diode series, having a plurality of serially connected diodes, wherein an anode thereof is coupled to the high-voltage supply rail and a cathode thereof is coupled to the node;

a second diode series, having a plurality of serially connected diodes, wherein a cathode thereof is coupled to the low-voltage supply rail and an anode thereof is coupled to the node; and

a first type MOS transistor, with a source region coupled to the high-voltage supply rail, a drain region coupled to the node and a gate coupled to the pre-driver; and

a second type MOS transistor, with a source region coupled to the low-voltage supply rail, a drain region coupled to the node and a gate coupled to the gate of the first type MOS transistor.

11. The ESD protection circuit according to claim 10, wherein when a voltage positive relative to the high-voltage supply rail is applied to the output pad, the ESD protection circuit provides a discharge path from the first diode to the high-voltage supply rail.

12. The ESD protection circuit according to claim 10, wherein when a voltage negative relative to the low-voltage supply rail is applied to the output pad, the ESD protection circuit provides a discharge path from the second diode to the low-voltage supply rail.

13. The ESD protection circuit according to claim 10, wherein when a voltage negative relative to the high-voltage supply rail is applied to the output pad, the ESD protection circuit provides a discharge path from the second diode, the second diode series and the first diode series to the high-voltage supply rail.

14. The ESD protection circuit according to claim 10, wherein when a voltage positive relative to the low-voltage supply rail is applied to the output pad, the ESD protection circuit provides a discharge path from the first diode, the first diode series and the second diode series to the low-voltage supply rail.

15. The ESD protection circuit according to claim 10, wherein each of the first diode, the second diode, the first diode series and the second diode series includes a non-gate diode formed by SOI fabrication process.

16. The ESD protection circuit according to claim 10, wherein each of the first diode, the second diode, the first diode series and the second diode series includes a non-gate diode formed by bulk CMOS fabrication process.

17. The ESD protection circuit according to claim 10, wherein the first and second diodes have the same dimension and the same junction capacitance.

18. The ESD protection circuit according to claim 10, wherein the first and second diodes have different dimensions and the different junction capacitances.

19. The ESD protection circuit according to claim 10, wherein the first type MOS transistor includes a PMOS transistor, and the second type transistor includes an NMOS transistor.

20. An ESD protection circuit of a non-gated diode, coupled between an input pad and an internal circuit, comprising:

a high-voltage supply rail and a low-voltage supply rail, coupled to the internal circuit;

a first diode and a second diode serially connected together, wherein an anode of the first diode is coupled to a node, and a cathode of the second diode is coupled to the high-voltage supply rail;

a third diode and a fourth diode serially connected together, wherein an anode of the third diode is coupled to the low-voltage supply rail a node, and a cathode of the fourth diode is coupled to the node; and

an ESD clamp circuit, coupled between the high- and low-voltage supply rails.

21. The ESD protection circuit according to claim 20, wherein the ESD clamp circuit comprises a plurality of serially connected diodes with an anode coupled to the high-voltage supply rail and a cathode coupled to the low-voltage supply rail.

22. The ESD protection circuit according to claim 20, wherein each of the first diode, the second diode, the third diode and the fourth diode includes a non-gate diode formed by SOI fabrication process.

23. The ESD protection circuit according to claim 20, wherein each of the first diode, the second diode, the third diode and the fourth diode includes a non-gate diode formed by bulk CMOS fabrication process.

24. The ESD protection circuit according to claim 20, wherein each diode of the ESD clamp circuit includes a non-gate diode formed by SOI fabrication process.

25. The ESD protection circuit according to claim 20, wherein each diode of the ESD clamp circuit includes a non-gate diode formed by bulk CMOS fabrication process.

26. The ESD protection circuit according to claim 20, wherein the first, second, third and fourth diodes have the same dimension and the same junction capacitance.

27. The ESD protection circuit according to claim 20, wherein the first, second, third and fourth diodes have different dimensions and the different junction capacitances.

28. A non-gated diode structure of a SOI, comprising:

a SOI substrate, comprising a substrate, an insulating layer and a silicon layer stacked in sequence;

a pair of isolation structures in the silicon layer to define a well region between the isolation structures in the silicon layer;

a first type doped region and a second type doped region located in the well region and adjacent to the isolation structures.

29. The non-gated diode according to claim 28, wherein the first type doped region and the second type doped region are implanted with P-type and N-type ions respectively.

30. The non-gated diode according to claim 28, wherein the well region is lightly implanted with a P-type ion.

31. The non-gated diode according to claim 28, wherein the well region is lightly implanted with an N-type ion.

32. The non-gated diode according to claim 28, wherein the insulating layer includes a buried oxide layer.

33. The non-gated diode according to claim 28, wherein the isolation structures include shallow trench isolations.

34. A non-gated diode structure of a SOI, comprising:

a SOI substrate, comprising a substrate, an insulating layer and a silicon layer stacked in sequence;

a pair of isolation structures in the silicon layer, and a first well region and a second well region neighboring to each other;

a first type doped region and a second type doped region respectively located in the first well region and the second well region, and adjacent to the isolation structures,

thereby a junction of the non-gate diode is the junction between the first and second well regions.

35. The non-gated diode according to claim 34, wherein the first type doped region and the second type doped region are implanted with P-type and N-type ions respectively.

36. The non-gated diode according to claim 34, wherein the first and second well regions are lightly implanted with a P-type ion and an N-type ion.

37. The non-gated diode according to claim 34, wherein the insulating layer includes a buried oxide layer.

38. The non-gated diode according to claim 34, wherein the isolation structures include shallow trench isolations.

39. A method of forming a non-gate diode of a SOI, comprising:

providing a SOI with a substrate, an insulating layer and a silicon layer sequentially stacked together;

forming a pair of isolating structures in the silicon layer, so as to define a well region therebetween;

forming a first type doped region and a second type doped region in the well region and adjacent to the isolating structures.

40. The method according to claim 39, wherein the first type and second type doped regions are implanted with P-type and N-type ions, respectively.

41. The method according to claim 39, wherein the well region is lightly implanted with a P-type ion.

42. The method according to claim 39, wherein the well region is lightly implanted with an N-type ion.

43. A non-gated diode structure in a CMOS process, comprising:

a substrate having a well region therein;

a pair of blocking isolation structures in the substrate;

a first type doped region located in the well region and between the blocking isolation structures; and

a pair of second type doped regions located in the well region and respectively adjacent to the blocking isolation structure, wherein each second type doped region is separated from the first type doped region by the well.

44. The non-gated diode according to claim 43, wherein the first type doped region and the second type doped region are implanted with P-type and N-type ions respectively.

45. The non-gated diode according to claim 43, wherein the well region is lightly implanted with a P-type ion.

46. A method of forming a non-gate diode in a CMOS process, comprising:

providing a substrate having a well region therein;

forming a pair of blocking isolation structures in the substrate;

forming a first type doped region located in the well region and between the blocking isolation structures; and

forming a pair of second type doped regions located in the well region and respectively adjacent to the blocking isolation structure, wherein each second type doped region is separated from the first type doped region by the well.

47. The method according to claim 46, wherein the first type doped region and the second type doped region are implanted with P-type and N-type ions respectively.

48. The method according to claim 46, wherein the well region is lightly implanted with a P-type ion.